**Lesson Plan**

**Name of Faculty :- POONAM SHARMA**

**Discipline :- Electrical Engineering**

**Semester :- 3RD Semester**

**Subject :- ANALOG AND DIGITAL ELECTRONICS**

**Lesson Plan Duration:- 15 Week**

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| **Week** | **Theory** | **Practical** |
| **1st** | **Lecture Day** | **Topic** | **Practical Day** | **Topic** |
| **1st** | **UNIT I****Semiconductor Devices**1.1 Concept of insulators, conductors and semiconductors. Intrinsic and extrinsicsemiconductor, P and N type semiconductor and their conductivity.  | **1st** | 1. To Plot V-I characteristics of a PN junction diode |
| **2nd** |  Effect of temperatureon conductivity of intrinsic semiconductor etc. |
| **3rd** |  PN junction diode, mechanism of current flow in PN junction | **2nd** | 1. To Plot V-I characteristics of a PN junction diode |
| **2nd** | **1st** | forward and reverse biasedPN junction, potential barrier, drift and diffusion currents, depletion layer. V-Icharacteristics of diodes.  | **1st** | 2. To Plot V-I characteristics of a Zener diode.. |
| **2nd** |  Diode as half-wave, full wave and bridge rectifiers |
| **3rd** | Peak InverseVoltage, rectification efficiencies and ripple factor calculations, | **2nd** | 2. To Plot V-I characteristics of a Zener diode.. |
| **3rd** | **1st** |  Concept of filters.  |  | 3. Observe the output of waveform:4. Half-wave rectifier circuit using one diode5. Full-wave rectifier circuit using two diodes6. Observe the output of waveform of Bridge-rectifier circuit using four diodes. |
| **2nd** | Typesof diode, characteristics and applications of Zener diodes. |
| **3rd** | REVISION CW checking | **2nd** | 3. Observe the output of waveform:4. Half-wave rectifier circuit using one diode5. Full-wave rectifier circuit using two diodes6. Observe the output of waveform of Bridge-rectifier circuit using four diodes. |
| **4th** | **1st** | **UNIT II: BIPOLAR-TRANSISTORS AND FIELD EFFECT TRANSISTORS**2.1 Concept of a bipolar transistor, PNP and NPN transistors.  | **1st** | 7. Plotting of input and output characteristics and calculation of parameters of transistors inCE configuration. |
| **2nd** | CB, CE, CC configurations ofa transistor. Comparison of CB, CE and CC Configurations.  |
| **3rd** | Transistor as an amplifier in CE Configuration, Current amplification factors, | **2nd** | 7. Plotting of input and output characteristics and calculation of parameters of transistors inCE configuration. |
| **5th** | **1st** | 2 Construction, operation and characteristics of FETs. | **1st** |  8. Plotting of input and output characteristics and calculation of parameters of transistors inCB configuration. |
| **2nd** | FET as an amplifier |
| **3rd** |  Construction,operation and characteristics of a MOSFET. Comparison of JFET, MOSFET andBJT. | **2nd** | 8. Plotting of input and output characteristics and calculation of parameters of transistors inCB configuration. |
| **6th** | **1st** | REVISION assignment | **1st** | 9. Plotting of V-I characteristics of a FET. |
| **2nd** | **UNIT III: DIGITAL ELECTRONICS**3.1 Distinction between analog and digital signal. Decimal, Binary, octal and hexadecimalnumber system  |
| **3rd** | Conversion from decimal and hexadecimal to binary and vice-versa. | **2nd** |  9. Plotting of V-I characteristics of a FET. |
| **7th** | **1st** | Binary addition and subtraction  | **1st** | 10. Basic logic operations of AND, OR, NOT gates. |
| **2nd** |  2 Definition, symbols and truth tables of Logic gates (AND, OR, XOR, NOT, NAND,NOR and XNOR). |
| **3rd** | NAND,NOR and XNOR). | **2nd** | 10. Basic logic operations of AND, OR, NOT gates.. |
| **8th** | **1st** | , REVISION CW checking | **1st** | 11. Verification of truth tables for NAND, NOR and Exclusive OR (EX-OR) and ExclusiveNOR (EX-NOR) gates. |
| **2nd** | .**UNIT IV: SEQUENTIAL AND COMBINATIONAL CIRCUIT** |
| **3rd** | 4.1 Half adder, Full adder, | **2nd** | 11. Verification of truth tables for NAND, NOR and Exclusive OR (EX-OR) and ExclusiveNOR (EX-NOR) gates. |
| **9th** | **1st** | Full adder, | **1st** | 12. Realization of logic functions with the help of NAND or NOR gates. |
| **2nd** | Full adder, |
| **3rd** | Mux, De-Mux, Encoder and Decoder. | **2nd** | 12. Realization of logic functions with the help of NAND or NOR gates. |
| **10th** | **1st** | Mux, De-Mux, Encoder and Decoder. | **1st** | 13. To design a half adder using XOR and NAND gates and verification of its operations.**-** |
| **2nd** | Latch, Flip Flops |
| **3rd** | Latch, Flip Flops | **2nd** | 13. To design a half adder using XOR and NAND gates and verification of its operations.**- do--** |
| **11th** | **1st** | shift registers. | **1st** | 14. Construction of a full adder circuit using XOR and NAND gates andverify its operation |
| **2nd** | shift registers. |
| **3rd** | counters. | **2nd** | 14. Construction of a full adder circuit using XOR and NAND gates andverify its operation |
| **12th** | **1st** | counters. | **1st** | 15. Verification of truth table for IC flip-flops (At least one IC each of D latch, D flip-flop,JK flip-flops). |
| **2nd** |  A/D and D/A Converters and its Applications. |
| **3rd** | A/D and D/A Converters and its Applications. | **2nd** | 15. Verification of truth table for IC flip-flops (At least one IC each of D latch, D flip-flop,JK flip-flops). |
| **13th** | **1st** | REVISION | **1st** | 16. Verification of truth table for encoder and decoder ICs. |
| **2nd** | REVISION |
| **3rd** | REVISION | **2nd** | 16. Verification of truth table for encoder and decoder ICs  |
| **14th** | **1st** |  | **1st** | 17. Verification of truth table for Mux and De-Mux.REVISION PRACTICAL |
| **2nd** | REVISION  |
| **3rd** | REVISION  | **2nd** | 17. Verification of truth table for Mux and De-Mux.REVISION PRACTICAL |
| **15th** | **1st** | REVISION  | **1st** | REVISION PRACTICAL |
| **2nd** | REVISION  |
| **3rd** | REVISION  | **2nd** | REVISION PRACTICAL |